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2D-Numerical Analysis of I_{DS}-V_{GS} Characteristic In pc-Si TFT's: Investigation of Inhomogeneous Structure

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Abstract

Transistors made of thin layers (Thin Film Transistor: TFT) are used primarily for the realization of active matrix flat panel displays liquid crystal. They constitute the basic element of a specific part of electronic known as "Large Surface Electronic".

The Poly-TFTs are made of a thin un-doped polycrystalline silicon film deposited on a glass substrate by the Low Pressure Chemical Vapor Deposition technique LPCVD; this choice limits the technological process to the temperature < 600°C. The benefit of pc-Si is to make devices with large grain size. Unfortunately, according to the conditions during deposition, the pc-Si layers can consist of a random superposition of grains of different sizes, where it appears grains boundaries parallels and perpendiculars.

In this paper, the transfer characteristics I_{DS}-V_{GS} are simulated by solving a set of two-dimensional (2D) drift-diffusion equations together with the usual density of states (DOS: exponential band tails and Gaussian distribution of dangling bonds) localized at the grains boundaries. The effect of density of intergranular and interface traps states, band to band tunneling (BBT), thickness of active layer, grain size and position of grain boundaries on the TFT's characteristics for a drain bias equal to 1V have been investigated.

keywords: Transistor TFT; 2D simulation; Heterogeneous structure; Grain size; Transfer characteristic.

1. Introduction

Transistors made of thin layers (Thin Film Transistor: TFT) are used primarily for the realization of active matrix flat panel displays liquid crystal [1]. For flat screens, it is impossible to integrate transistors on a monocrystalline silicon wafer in the pixel array for technology reasons. On one hand, the maximum size of the wafer cannot exceed about 30 cm while it is now standard for flat screens to work on substrates of more than 2m [2]. On the other hand, the substrate of the transistor in monocrystalline silicon is typically conductor while that of TFTs is therefore glass or plastic insulation. In addition, the maximum temperature of the manufacturing process of monocrystalline silicon transistors is about 1000 ° C while that of the TFTs is a few hundred ° C, which is compatible with glass substrates with low cost or even some plastic substrates.

At present, the TFTs are mostly made of the hydrogenated amorphous silicon (a-Si:H) [3]. This material may indeed be deposited on large surfaces in low temperature (T = 200 °C). The choice of this temperature is dictated by the desire to use inexpensive glass substrates. The insufficient electrical

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properties of this material limited the use of TFT (a-Si: H) in pixels. The control circuits of the matrix in this case are realized of monocrystalline silicon outside the glass substrate. The necessity for a connection between the matrix and the control circuits causes therefore an increase in weight, size, cost of the device and reduced reliability. The connection between the two entities mentioned above becomes very difficult. The electrical properties of polysilicon much higher than amorphous silicon, allow its use in transistors of pixels and in the control circuits also. The main objective of this paper is to use a program based on the numerical solution of two-dimensional equations (Poisson equation and the two equations of continuity of electrons and holes) to study the impact of density of intergranular traps states, Band to band tunneling (BBT), grain size and position of grain boundaries on the TFT's transfer characteristics I_{DS}-V_{GS} for a drain bias equal to 1V.

2. Modeling Description

The structure of polycrystalline silicon is highly dependent on technology used to form the material. When the polycrystalline film is obtained after solid phase crystallization of amorphous silicon film, its structure is columnar. The crystallized material is assumed formed by parallel single-crystalline grains, L_G sized, separated by physically thick amorphous grain boundaries with a thickness of 1 nm.

2.1. Simulated structure

Figure 1 shows the geometrical model adopted in the two-dimensional simulation of the poly-Si TFT's where the grain boundaries are perpendicular to the growth surface. Because of the complexity of the structure model and the limited number of points in programming language, only five perpendicular grain boundaries are considered here. The geometrical model assumes that Poly-Si layer is composed by crystalline grains separated by amorphous silicon transition zones commonly called grain boundaries which are perpendicular to the growth surface and which include the usual density of states (DOS) with exponential band-tails and Gaussian distributed deep levels. All simulations are performed for a grain size L_G of 300 nm, a thickness of 150 nm and drain bias V_{DS} equal to 1V.

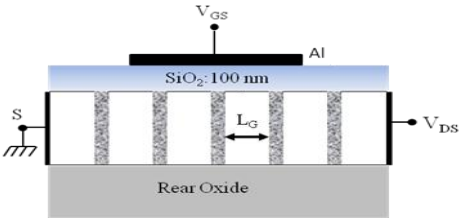

Fig. 1. Two dimensional geometrical of poly-Si TFT's

2.3 Electrical conduction

Simultaneous numerical resolution of the coupled Poisson (1), electron (2) and hole (3) continuity equations are numerically solved in two dimensions:

$$\nabla\left(\varepsilon_S \nabla\Phi(x,y)\right) = -\ q(p(x,y) - n(x,y) + N_D - N_A + \sum N_T(x,y)) \qquad (1)$$

$$\nabla J_n = qU\left(\Phi(x,y), \Phi_n(x,y), \Phi_p(x,y)\right) \quad (2)$$

$$\nabla J_p = -qU\left(\Phi(x,y), \Phi_n(x,y), \Phi_p(x,y)\right) \quad (3)$$

The electron and hole conduction currents, J_n and J_p , are then given by:

$$J_n(x,y) = -qn(x,y)\mu_n \nabla\left(\Phi_n(x,y)\right) \quad (4)$$

$$J_p(x,y) = -qp(x,y)\mu_p \nabla\left(\Phi_p(x,y)\right) \quad (5)$$

In these equations, the symbols used are:
ε_s: The permittivity of silicon material;
$n(p)$: The free electrons (holes) density;
Φ, Φ_n, Φ_p : The electrostatic potential, the electron and hole electrochemical Fermi potentials;
μ_n, μ_p : The band microscopic electron and hole mobilities;
N_D (N_{AS}) : The ionized donor (acceptor) density;
$\sum N_T$: The sum of the different trap states present in the material.
In the both continuity equation, U represents the net active generation-recombination rate.
Due to the non-linearity of the three coupled partial equations of the system formed by the first three equations, the determination of unknown Φ, Φ_n , Φ_p values requires a numerical method. We have used the standard finite difference defined by Gummel's decoupling method [4]. Therefore, each equation is discretized on a variable mesh (strongly refined at interface and grain boundaries) then linearized to the first order. The numerical resolution is based on the method of relaxation by line and by column. The tridiagonal character of the matrix leads us to use the Gauss's elimination method.
The Hypotheses and parameters values of the density of states in the grain boundaries are the same that reported in reference [5].

2.2. Density of states at the grain boundaries

The usual density of states (DOS) model in the amorphous silicon is used to describe the distribution of the states inside the forbidden band-gap of the amorphous grain boundaries. It is consisted of two decreasing exponential distributions for the valence and the conduction band tail and two correlated Gaussian distributions for deep defects introduced by dangling bonds.

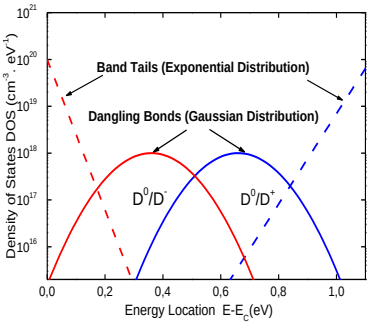

Fig. 2. Density of States (DOS) in the gap of the amorphous grain boundaries regions

3. Results of 2D-numerical simulation

A. Effect of intergranular density of states

The presence of intergranular traps states in the band gap increases the value of the current I_{OFF} (Fig. 3). This change is explained by the fact that these traps states will behave in the blocking state as states permit, they will facilitate the transition of carriers from one band to another by creating a gateway intermediary for conduction, significantly increasing the current of the transistor in the blocking state. The carriers will no longer need to spend energy of 1.12eV to pass from a band to another but they can do that with small successive jumps requiring a lower energy for each jump. Thus the creation electron-hole pairs will be assisted by the allowed states in the band.

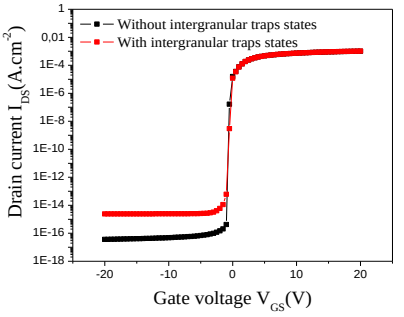

Fig. 3. Simulated transfer characteristics I_{DS} (V_{GS}) with and without density of intergranular traps states in poly-Si TFT's.

B. Effect of grain size

Since the granular structure of the active layer has a direct influence on the transfer characteristic of the TFT Poly-Si, we are interested to represent more closely in Fig.4, the evolution of the drain current as a function of gate voltage for several grain sizes L_G ranging from 0.15 µm to 1µm.

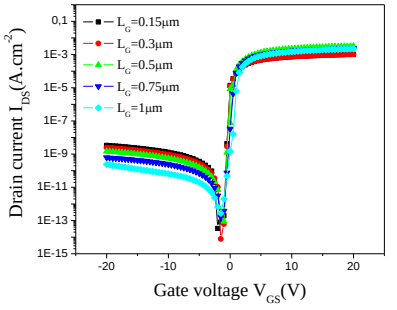

Fig. 4. Effect of grain size on the transfer characteristics I_{DS}-V_{GS} in poly-Si TFT's.

We note that in regime of accumulation the drain current I_{DS} is a little affected by the grain sizes. This is due to an important contribution of electron by the tension V_{GS} that fills those trapped in the grain boundaries by a lowering of the intergranular barrier. In regime of inversion, the current decreases with the increasing of grain sizes. It was shown that the process of growth of grain improves the physical and electrical properties of poly-Si layers and consequently devices made from it [6].

C. Effect of position of grain boundaries

Figure 5 shows the effect of the first grain boundary near the drain contact X_{jG1} in the drain current I_{DS} as a function of V_{GS} :

$$X_{jG1} = L_C - (n_{jG}-1)\times L_G$$

L_C: The channel thickness;
n_{jG} : The number of grain boundaries;
L_G : The grain size.

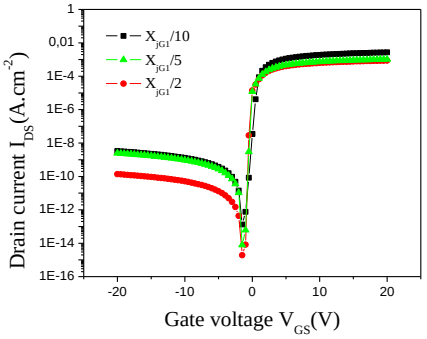

Fig. 5. Effect of position of the first grain boundary near the drain contact on the transfer characteristics I_{DS}-V_{GS} in poly-Si TFT's.

For a positive gate voltage (V_{GS} >0), the change of the position of grain boundary has a slight influence on the level of the density of drain current I_{DS} ,on the contrary we can see that this influence is significant for negative voltages. The increase in reverse current due to the band to band tunneling is mainly due to the amplification of emission factor for electric field in which the place of the main issue is the first grain boundary near the drain.

4. Conclusions

In this paper, a numerical modeling was developed to simulate the effect of grain boundaries in the characteristic electric of Poly-Si TFT's.
It has been found that:
- The introduction of intergranular traps states causes a shift of the characteristic I_{DS} (V_{GS}) . However, the reverse current tends to increase with V_{GS} ;
- The effect of density of intergranular traps states is important just for a negative gate voltage;

- Trap states behave in the blocking state as states permit that will facilitate the transition of carriers from one band to another by creating through a gateway for the conduction ;
- The introduction of intergranular traps states increases just the current I_{OFF} .

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