Macromodeling of Power MOSFET Transistor Incorporating Self-Heating Effect

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Abstract –

An empirical self-heating SPICE MOSFET model which accurately portrays the vertical DMOS power MOSFET electrical and thermal responses is presented. This macromodel implementation is the culmination of years of evolution in MOSFET modeling. This new version brings together the thermal and the electrical models of a VDMOS MOSFET. The existing electrical model is highly accurate and is recognized in the industry. Simulation responses of the new self-heating MOSFET model track the dynamic thermal response independently of SPICE's global temperature definition. Existing models may be upgraded to self-heating models with relative ease.

Keywords – Device characterization, device modeling, high power discrete devices, modeling, MOS device, power semiconductor devices, semiconductor devices, simulation, Spice, thermal design**.**

I. INTRODUCTION

Many of the power MOSFET models available today are based on an ideal lateral MOSFET device. They offer poor correlation between simulated and actual circuit performance in several areas. They have low and high current inaccuracies that could mislead power circuit designers. This situation is further complicated by the dynamic performance of the models. The ideal low power SPICE level-1 NMOS MOSFET model does not account for the nonlinear capacitive characteristics Ciss, Coss, Crss of a power MOSFET. Higher level SPICE MOSFET models may be used to implement the non-linear capacitance with mixed results. The inherent inaccuracies of modeling a power VDMOS with the SPICE MOSFET model dictated the need for an alternative approach; a macro-model.

A macro-model such as the one defined by Wheatley and Hepp [1] can address the short comings of the ideal low power SPICE MOSFET model. Highly accurate results are possible by surrounding the ideal MOSFET model with resistive, capacitive, inductive and other SPICE circuit elements. Two examples will illustrate the approach:

1) It was demonstrated in [3] that a third parallel MOSFET is required to accurately model the exponential relationship of drain current and gate to- source voltage in the sub-threshold region

2) The implementation of the network (figure 1) using switches S1 and S2 provided a method to precisely model the non-linear capacitance. The result is an accurate representation of the dynamic transition between blocking and conduction. The need for this higher level modeling accuracy becomes apparent in high frequency applications where gate charge losses as a proportion of overall losses become significant. The same situation exists for the space charge limiting effect at high drain current.

The MOSFET model reference on which this work is based has been explained in [1]-[2]-[3]. The reader is encouraged to refer to these references for a full understanding of the MOSFET model parameters herein referred to as the standard SPICE MOSFET model. Recent works [8]-[9] have demonstrated methods of circumventing the SPICE global temperature definition, providing a means of using the device's own junction temperature as a self-heating feedback mechanism.

The model developed in [8] has limitations involving proprietary algorithms, rendering the method of limited interest. Model implementation is convoluted, involving an analog behavioural MOSFET model (ABM) whose operating characteristics are dependent on a SPICE level-3 NMOS MOSFET. As a result, both the switching circuit and the load must be duplicated for the model to function. The implementation in [9] does not model the drain-source avalanche property of a MOSFET. Neither [8] nor [9] attempt to model the temperature characteristics of the intrinsic body diode.

II.   STANDARD SPICE MOSFET MODEL

The macro-model in Figure 1 is that used in many Fairchild MOSFET device models. It is the evolution of many years of work and improvements from numerous contributors [1]-[7]. A significant advantage of this model is that extensive knowledge of device physics or process details are not required for implementing parametric   data   within   the   model.

The following data curves are the basis used to generate the macro-model model over temperature: transfer characteristic, saturation characteristic, Rds (on), gate threshold voltage, drain-to-source breakdown voltage, intrinsic body diode voltage, capacitance versus drain-to-source voltage, and gate charge waveform. Parametric data for up to five temperature points are used for model calibration resulting in a macro-model that provides representative simulation data for any rated operating junction temperature. The limitation of the standard MOSFET model is found in simulations involving severe pulsed power dissipation, and parallel operation. Reliance of the SPICE MOSFET primitive on the global analysis temperature variable (.TEMP SPICE instruction) results in simulations having all MOSFETs operating at a single predefined temperature. Device behavior under high power dissipation transitory excursions cannot be accurately modeled. Threshold voltage and Rds(on) are but two of the important parameters that can change sufficiently as to render a simulation inaccurate
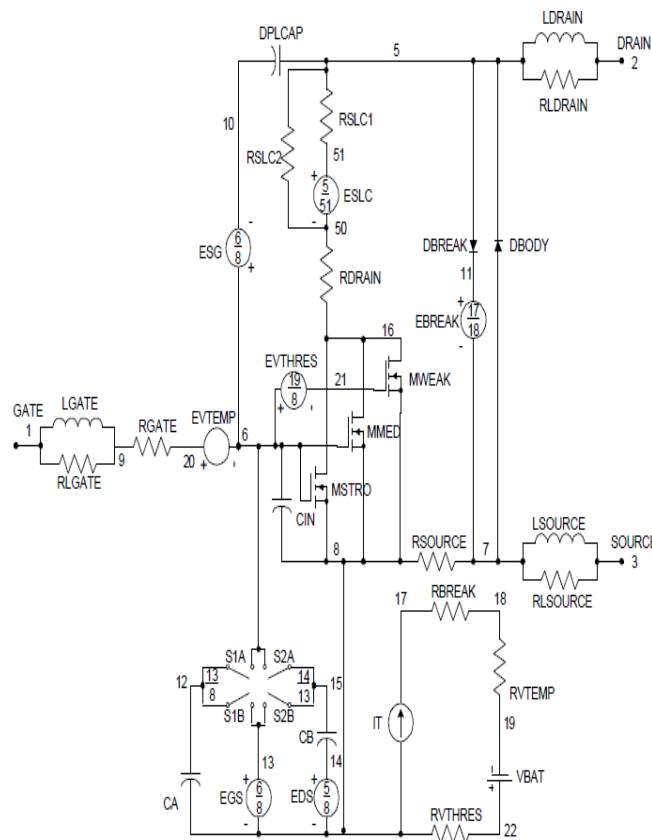

Figure.1 Standard MOSFET Macro-model Dependent on Global Temperature Definition

III.   Self-Heating Spice MOSFET Model

Improved implementation of static and dynamic behaviour is achieved with the self-heating SPICE MOSFET model (Figure 2), an evolution of the standard MOSFET model (Figure 1). Improved implementation of static and dynamic behaviour is achieved. Temperature dependent model parameters respond in closed loop form to the junction temperature information provided by node Tj. Performance is independent of SPICE's global temperature definition .TEMP, circumventing the level-1 NMOS model primitive self-heating limitation. All MOSFET operating losses are inclusive in the current source G_Pdiss (scaling of 1A = 1W dissipation) representing instantaneous power dissipation into the thermal model.

Multiple MOSFETs may be simulated at different and variable junction temperatures. Each MOSFET can be connected to a heat sink model via node Tcase. The heat sink model can be device specific, so heat sink optimization becomes possible. Current source G_Pdiss is referenced to the simulation ground reference, permitting use of the model in bridge topologies
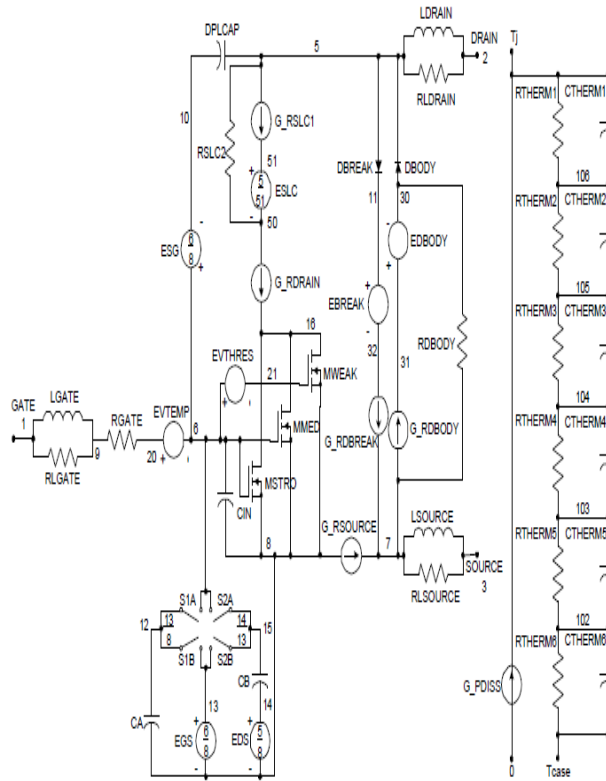

Figure.2 Self-Heating MOSFET Macro-model Independent of Global Temperature Definition

An example of a symbol representation of the self-heating MOSFET model is shown in Figure 3. Symbol files are available for OrCAD's two circuit entry tools "PSpice Schematic" and "OrCAD Capture". Recommended implementation of the symbol is to designate the pin out attribute for Tj as optional (ERC = DON'T CARE). Tj is the representation of the device junction temperature. It may be used as a monitoring point, or it may be connected to a defined voltage source to override the self-heating feature. Tcase must be connected to a heat sink model. Treatment of connections to the model's gate, drain, and source terminals are no different than those of the standard MOFET model.
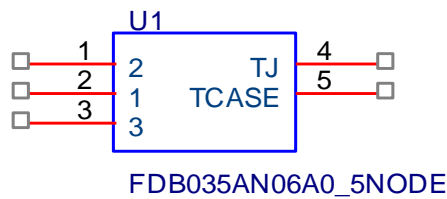

Figure.3 Self-Heating Power MOSFET PSPICE Symbol

IV.   SELF-HEATING MODEL IMPLEMENTATION

Ability to describe the value of a resistor and its temperature coefficients as a behavioural model referenced to a voltage node is necessary to express dependence on junction temperature. SPICE resistor ABMs do not permit voltage node references. Dynamic temperature dependence of the MOSFET's resistive element (expressed as separate lumped elements) and of the diode's resistive component cannot be implemented without a resistor behavioural model. This limitation is overcome by using a voltage controlled current source ABM expression (Figure 4). By using the nodes of the current source for voltage control, it becomes possible to express a resistor as a voltage-controlled current source by implementing the expression for the resistor's current as I = V/R (Tj). The resistance R (Tj) becomes a behavioural model expression dependent on the voltage node Tj representation

of junction temperature. This voltage-controlled current source ABM model was used to modify the standard MOSFET model from Figure 1 by implementing voltage dependent versions of RDRAIN, RSOURCE, and RSLC1. Behavioural expressions were implemented in the self-heating model to eliminate IT, RBREAK, RVTEMP, and V_{BAT} through modification of EVTEMP, EVTHRES, and EBREAK.
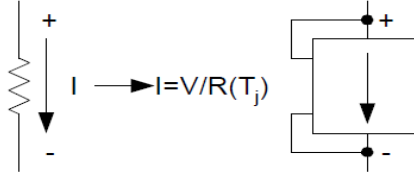

Figure.4 Implementing a Voltage Dependent ABM Resistor Model

Temperature dependent resistive elements of diodes DBODY and DBREAK were separated from the diode model and expressed as voltage controlled current source ABM models G_R$_{DBODY}$ and G_R$_{DBREAK}$. A large value resistor R$_{DBODY}$ was added to improve convergence. ED$_{BODY}$ is added in series with D$_{BODY}$ to incorporate the intrinsic body diode forward conduction drop temperature dependency. Junction temperature information is implemented by the inclusion of the thermal network Z$_{\theta JC}$ and current source G_P$_{DISS}$. The thermal network parameters are supplied in Fairchild data sheets. G_P$_{DISS}$ calculates the MOSFET instantaneous operating loss, and expresses the result in the form of a current using the scaling ratio of 1A=1W. This is a circuit form implementation of the junction temperature from expression (1)

$$T_J = P_{Dissipation} + Z_{\theta JC} + T\ case \qquad (1)$$

Where T_J = junction temperature, $P_{Dissipation}$ = instantaneous power loss, $Z_{\theta JC}$ = thermal impedance junction-to-case and Tcase = Case temperature. Tj and Tcase use the scaling factor $1V = 1^oC$.

V.   SIMULATING UNCLAMPED INDUCTIVE SWITCHING

The unclamped inductive switching (UIS) test circuit in Figure 5 was used to compare the performance of the VDMOSFET (3.5 mΩ, 60V, TO-263) self-heating MOSFET model with that of the standard model and measurement results.
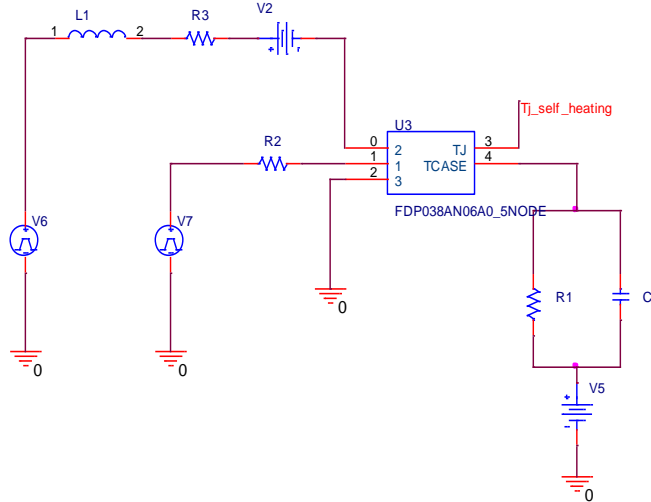

Figure.5 UIS circuit used in the simulation

The standard MOSFET model unclamped inductive switching simulation results were performed with PSPICE TNOM and .TEMP variables set to 25^oC (Figure 6). The lack of temperature feedback to the model results in a drain-source breakdown voltage that is strictly drain current dependent.
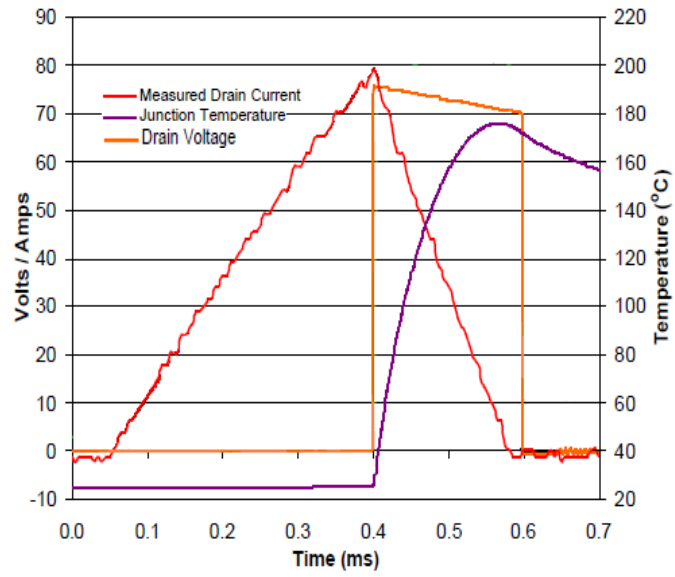
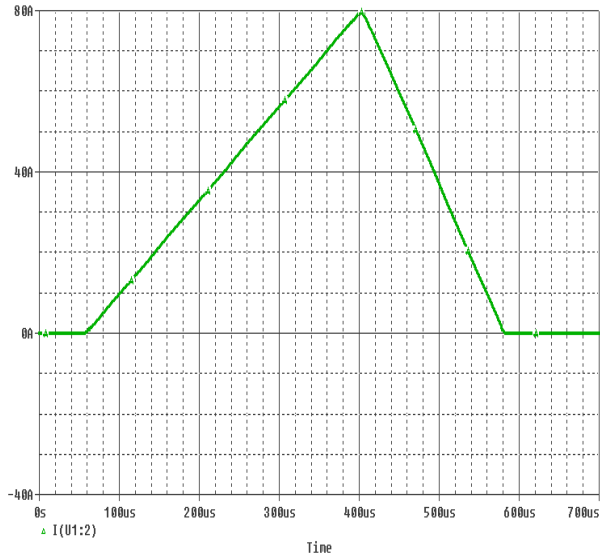Figure.6   Measured UIS waveforms for a Power MOSFET standard model

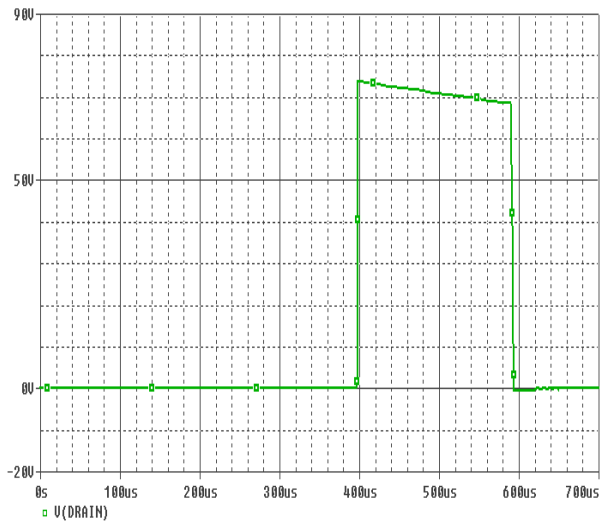Figure 6.a Simulated drain current for the Power MOSFET transistor

Figure.6.b Simulated drain voltage for the Power MOSFET transistor without self heating effect
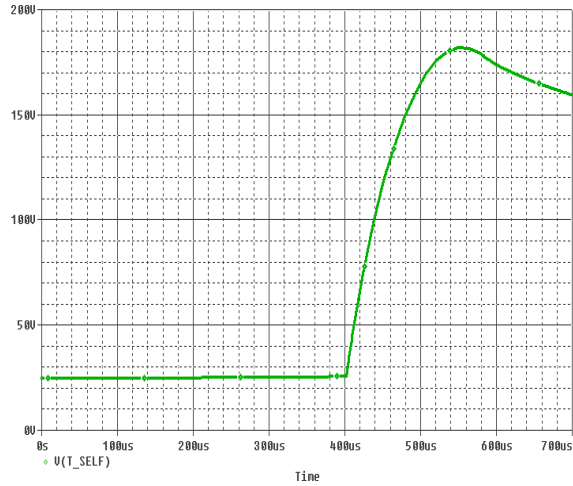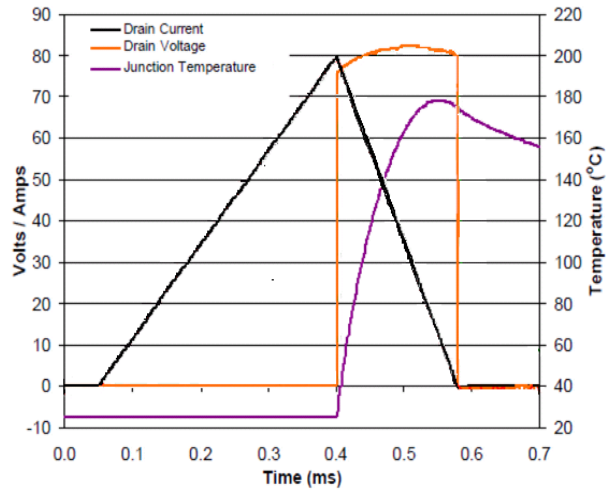
Figure.6.c. Simulated junction temperature

Figure.7 Measured UIS waveforms for a Power MOSFET Self-Heating Model

Unclamped inductive simulation results for a self heating MOSFET model are shown in Figure7. (a, b, c). Simulated drain-source breakdown voltage demonstrates the model dependence on junction temperature as well as drain current. Excellent agreement exits.
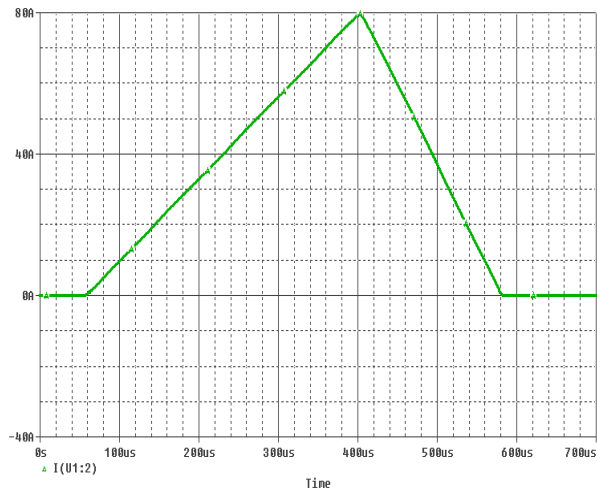

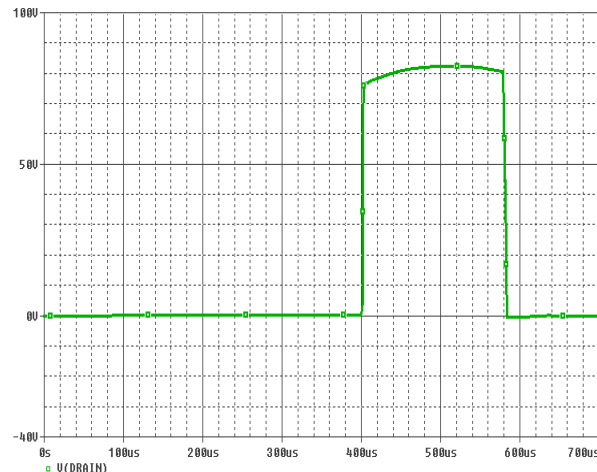Figure.7.a Simulated drain current for the Power MOSFET transistor

Figure.7.b Simulated drain Voltage for the Power MOSFET transistor with self heating effect
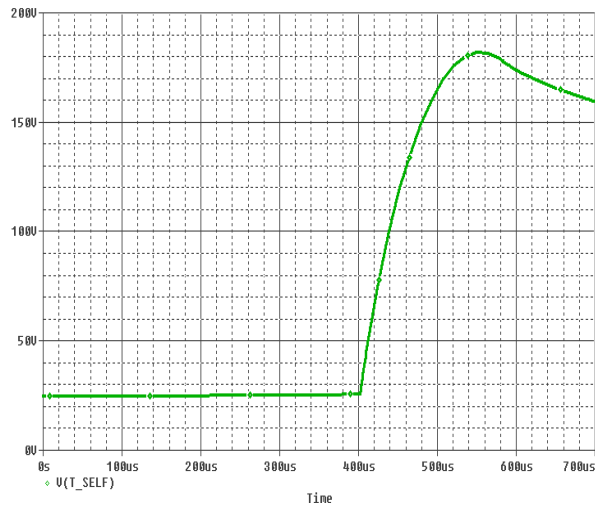
Figure.7.c Simulated Junction temperature for Power MOSFET transistor

VI.   SIMULATION CONVERGENCE

The self-heating model was tested under numerous circuit configurations. It was found to be numerically stable. Failure to converge can occur under some large signal simulations if PSPICE's setup option ABSTOL setting is less than 1μA. UIS simulations were performed on a Dell Latitude CSx using a 3.8GHz Pentium IV processor with 1GB of memory. Windows XP was the operating system used (virus scan software enabled). PSPICE Schematics version 10.5 was used

Simulation time results were:
- Standard model = 7.9s
- Self-heating model = 13.7s

Simulation time is expected to be longer with the self-heating model due to the dynamic interaction of the junction temperature feedback.

VII.   FUTURE MODEL DEVELOPMENTS

Minor inaccuracy is introduced if previously published Fairchild Semiconductor MOSFET models are modified to become self-heating models, but are within device tolerance. The inaccuracy can be eliminated by including the variable T_ABS=25 in the level-1 NMOS MOSFET and the intrinsic body diode models during device specific model calibration, permitting full compatibility of the model with the new self-heating model. This term was included for the standard MOSFET model calibration of the Power MOSFET.

VIII.   CONCLUSION

The self heating PSPICE power MOSFET macromodel provides the next evolutionary step in circuit simulation accuracy. The inclusion of a thermal model coupled to the temperature sensitive MOSFET electrical parameters results in a self-heating PSPICE power MOSFET macromodel which allows increased accuracy during time domain simulations. The effect of temperature change due to power dissipation during time domain simulations can now be modeled.

REFERENCES

[1]   Z. Bencic Jakopovi, "Identification of Thermal Equivalent- Circuit Parameters for Semiconductors". 2nd IEEE Workshop on Computers in Power Electronics, Bucknell University, USA, 6-7. August 2008., ISBN 0-87942-572-1, pp. 251–260

[2]   C.F. Wheatley, Jr., H.R. Ronan, Jr., and G.M. Dolny, "Spicing-up SPICE II Software For Power MOSFET Modeling," Fairchild Semiconductor, Application Note AN7506, February 2006.

[3]   F. Di Giovanni, G. Bazzano, A. Grimaldi,"A New PSPICE Power MOSFET Subcircuit with Associated Thermal Model", PCIM 2008 Europe, pp. 271-276.

[4]   C.F. Wheatley, Jr. and H.R. Ronan, Jr., "Switching Waveforms of the L 2 FET: A 5Volt Gate Drive Power MOSFET,"

[5]   D. T. Zweidinger, S. G. Lee, R. M. Fox, "Compact Modeling of BJT Self-Heating in SPICE", IEEE Transactions on Computer-Aided Design of IC and Systems, Vol. 12 No. 9, pp.1368-1375, 2003.

[6]   A. Hefner, "Simulating the dynamic electrothermal behaviour of power electronic circuits and systems", IEEE Transactions on Power Electronics, V0l.8, No.4, Oct. 1993.

[7]   Szekely, V., Van Bien, T., "Fine Structure of Heat Flow Path in Semiconductor Devices: Measurement and Identification Method," Solid-State Electronics,Vol. 31 (2002), pp. 1363-1368.

[8]   2] P. Nance, M. Marz, Thermal Modelling of Power Electronic System. PCIM Europe, 2/2000, pp. 20–27.

[9]   A. Maxim, D. Andreu, J. Boucher, "SPICE electrothermal modeling of power integrated circuits", IEEE MIEL'97 Conference.

[10]   Apendoorn, S. Schmitt, H.W. DE Donker, "An electrical model of a NPT-IGBT including transient temperature effects realized with PSPICE Device Equations modeling", Proceeding of IEEE ISIE'97 Conference, pp. 223-228.

[11]   A. Maxim, D. Andreu, J. Boucher, "SPICE electrothermal modeling of power integrated circuits", IEEE MIEL'97 Conference, pp. 479-482, 2005

[12]   Q. Chen, X. Yang, Z. Wang, L. Zhang, and M. Zheng, "Thermal design considerations for integrated power electronics modules based on temperature distribution cases study," in IEEE PESC Rec., Orlando, FL, Jun. 17–21, 2007, pp. 1029–1035.